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Edward W. Bulchis, Esq.
DORSEY & WHITNEY LLP
Suite 3400
1420 Fifth Avenue
Seattle, WA 98101

EXAMINER	
WALTER, CRAIG E	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 12/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/690,810	MEYER ET AL.	
	Examiner	Art Unit	
	Craig E. Walter	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-47* is/are pending in the application.

4a) Of the above claim(s) *39-47* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4, 8-19,21,23-29,33-38* is/are rejected.

7)☒ Claim(s) *5-7,20,22 and 30-32* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2/24/04, 8/16/04, 4/25/05, 8/22/05, 7/19/05, 6/23/05, 11/19/04, 4/29/04, 10/20/03, 4/15/05
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-38, drawn to a memory hub (module and system) capable of receiving and storing downstream memory responses, classified in class 711, subclass 118.

II. Claims 39-47, drawn to a method of forwarding memory responses of a memory system in a predetermined order, classified in class 711, subclass 158.

2. The inventions are distinct, each from the other because of the following reasons:

3. Inventions I and II are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention I has separate utility from invention II such as use in a system capable of multiplexing an output response selected from one of the plurality of queues used to store memory responses. See MPEP § 806.05(d).

4. Because these inventions are distinct for the reasons given above and the search required for any one invention (i.e. invention I) is not required for invention II, restriction for examination purposes as indicated is proper.

5. Applicant (Kimton Eng) elected group I without traverse during a telephonic interview held on 2 December 2005. Mr. Eng agreed to cancel the remaining claims (claims 39-47).

Information Disclosure Statement

6. The ten information disclosure statements (IDS) submitted on 24 February 2004, 16 August 2004, 25 April 2005, 22 August 2005, 19 July 2005, 23 June 2005, 19 November 2004, 1 June 2004, 29 April 2004, and 20 October 2003 have been fully considered by the Examiner.

7. The information disclosure statement filed on 15 April 2005 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each cited foreign patent document; each non-patent literature publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered. Specifically, the following two documents are not present in Applicant's file (as presented on page 5 of 5 of the PTO-1449 Form):

Intel, "Flash Memory PCI Add-In Card for Embedded Systems ..."

Shanley, T. et al., "PCI System Architecture, ..."

Drawings

8. The drawings received on 20 October 2003 are acceptable to the Examiner.

Specification

9. The abstract of the disclosure is objected to because extraneous markings are present (i.e., H:\IP\Documents\...as filed.doc). Correction is required. See MPEP § 608.01(b).

Claim Objections

10. Claims 1-8, 10-13, 16-22, 26, 29-32 and 36 are objected to because of the following informalities:

As for claim 1, the word "inform" should be changed to "from" in line nine.

As for claim 11, the word "a" in line three should be added between the word "or" and "bypass".

As for claims 16, 26 and 36, acronyms (such as SDRAM in claim 16) should not be used to abbreviate key words or phrases until they are explicitly defined (i.e. written in expanded form) previously within the claim itself, or a claim from which it depends.

As for claims 18 and 28, it is of the Examiner's opinion that Applicant intended claim 18 to depend on 16 (rather than 17), and claim 28 to depend on 26 (rather than 27) for the following reason:

> Claims 17 and 27 recite outputting memory responses stored in the local queue prior to memory responses stored in the buffered queue. Claim 18 and 28 recite outputting memory responses stored in the buffered queue prior to memory responses stored in the local queue. It is not possible to output one set of responses (i.e. buffered queue) first, then the other (local queue), and subsequently output the second, prior to the first. The claims will be further treated on their merits based on the aforementioned assumption.

Claims 2-8, 12-13, 17-22 and 29-32 further limit one of the aforementioned claims therefore they too are objected to.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

11. Claims 1-4, 9-13 and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Bogin et al., hereinafter Bogin (US Patent 6,523,093 B1).

As for claims 1 and 15, Bogin teaches a memory hub (as in claim 1 and a memory module in claim 15), comprising:

a plurality of memory devices (L1 and L2 cache (Fig. 1, elements 106 and 108 respectively));

a memory hub coupled to the memory devices (Fig. 1, element 112), the memory hub including,

a local queue adapted to receive local memory responses, and operable to store the local memory responses (Fig. 2, element 210 – a write cache inherently receives and stores memory responses);

a bypass path adapted to receive downstream memory responses, and operable to pass the downstream memory responses (Fig. 2, element 128 – the memory controller creates a bypass path from the main memory (element 132 not shown in Fig. 2) to the mux (element 220), i.e. downstream, without having to store the memory response in the prefetch buffer);

a buffered queue coupled to the bypass path and operable to store downstream memory responses (Fig. 2, element 126, the prefetch buffer is coupled to the memory controller. Again, a prefetch buffer inherently stores memory responses, in this instance, downstream from the main memory) – col. 5, lines 24-28;

a multiplexer coupled to the local queue, buffered queue and bypass path, the multiplexer being operable to output responses inform a selected one of the queues or the bypass path responsive to a control signal (the mux can output one of the three responses (either from the prefetch buffer, the bypass path (memory controller) or the write cache) and output it to the processor bus controller (element 114)). A control signal (element 222) is provided from the read request queue (element 214) which selects one of the three aforementioned signals (col. 3, lines 33-43); and

arbitration control logic coupled to the multiplexer, the arbitration logic operable to develop the control signal to control the selection of

responses output by the multiplexer (again, the read request queue generates the control signal (222) to select one of the three responses (col. 3, lines 33-43).

As for claim 2, Bogin teaches the memory hub of claim 1 wherein the arbitration control logic develops the control signal to output memory responses stored in the local queue prior to memory responses stored in the buffered queue (col. 3, lines 24-45, read requests are sent from the processor via the processor bus controller to the read request controller (Fig. 2, element 206). If the read request controller selects an entry in the write cache, the control signal (element 222) will instruct the mux to output the memory responses from the write cache prior to any requests from the prefetch buffer).

As for claim 3, Bogin teaches the memory hub of claim 1 wherein the arbitration control logic develops the control signal to output memory responses stored in the buffered queue prior to memory responses stored in the local queue (col. 3, lines 24-45, read requests are sent from the processor via the processor bus controller to the read request controller (Fig. 2, element 206). If the read request controller selects an entry in the prefetch buffer, the control signal (element 222) will instruct the mux to output the memory responses from the prefetch buffer prior to any requests from the write cache).

As for claim 4, Bogin teaches the arbitration control logic as developing the control signal to provide the memory responses from the local and buffered queues as a function of the age of a memory request associated with each memory response (col. 5, lines 48-67, Bogin discusses assigning an age value to each entry in the buffers. The least recently used logic is then implemented to assign ages to the entry, hence limiting

the amount of time it can be stored in the buffer before is read out (as selected by the read request controller).

As for claim 9, Bogin teaches a memory hub adapted to receive local memory responses and downstream memory responses, the memory hub operable to store the received memory responses and operable to apply an arbitration algorithm to select the order in which the stored local and downstream memory responses are provided on an uplink output (Fig. 2 depicts a memory control hub comprising a prefetch buffer, element 126 (buffered queue), and a write cache, element 210 (local queue). A read request queue (element 214) sends a control signal (element 222) to a mux in order to select memory locations from one of the two queues to upload (i.e. provide to an uplink output) to a processor bus controller (element 114). Again referring to col. 3, lines 33-43, the mux is programmable to provide data from one of the queues to the uplink. The mux uses the generated control signal to select memory locations from one of the queues. The control signal is accompanied with a token (element 224) which helps select the memory location to forward to the mux (i.e. arbitration algorithm) as an arbitration algorithm is simply a protocol used to arbitrate between two or more competing resources - (col. 3, lines 43-52).

As for claim 10, Bogin teaches the memory hub of claim 9 wherein the memory hub further comprises a local queue that stores the local memory responses (Fig. 2, element 210 – a write cache inherently receives and stores memory responses) and a buffered queue that stores the downstream memory responses (Fig. 2, element 126, the

prefetch buffer which buffer inherently stores memory responses, in this instance, downstream from the main memory).

As for claim 11, Bogin teaches the memory hub of claim 10 wherein the memory hub further comprises a multiplexer coupled to the local queue, buffered queue, and bypass path, the multiplexer providing responses from one of the queues or a bypass path on an output responsive to a control signal (the mux can output one of the three responses (either from the prefetch buffer, the bypass path (memory controller) or the write cache) and output it to the processor bus controller (element 114)). A control signal (element 222) is provided from the read request queue (element 214) which selects one of the three aforementioned signals (col. 3, lines 33-43)..

As for claim 12, Bogin teaches the memory hub of claim 11 wherein the memory hub further comprises arbitration logic coupled to the queues and the multiplexer, and wherein the arbitration logic applies the control signal to the multiplexer to control which memory responses are provided on the output (again, the read request queue, coupled to the queues and mux, generates the control signal (222) to select one of the three responses (col. 3, lines 33-43)).

As for claim 13, Bogin teaches the memory hub of claim 12 further including a bypass path coupled to the buffered queue and coupled to the multiplexer, the bypass path adapted to receive the downstream memory responses and operable to provide the responses to the multiplexer and the buffered queue (Fig. 2, element 128 – the memory controller creates a bypass path from the main memory (element 132 not shown in Fig. 2) to the mux (element 220), i.e. downstream, without having to store the

memory response in the prefetch buffer. The controller is further coupled to the prefetch buffer).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 24, 26-29, 34 and 36-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Talbot et al., hereinafter Talbot (US PG Publication 2005/0166006 A1) in further view of Bogin.

As for claim 24, Talbot teaches a computer system, comprising:

a memory hub controller (Fig. 1, element 105);

a plurality of memory modules (Fig. 1, elements 150A-150B) , each memory module being coupled to adjacent memory modules through respective high-speed links (Fig. 1, elements 110B and110C – paragraph 0034, lines 1-5), at least one of the memory modules being coupled to the memory hub controller through a respective high-speed link (Fig. 1 depicts the high-speed uplink and downlinks (elements 111A and 112A respectively) coupled to the hub controller), and each memory module comprising:

a plurality of memory devices (Fig. 2, element 261A through 261N); and

a memory hub coupled to the memory devices (Fig. 1, element 112).

Though Talbot teaches a memory hub, he fails to teach the memory hub as claimed by Applicant. Bogin however teaches a memory hub comprising,

a local queue adapted to receive local memory responses, and operable to store the local memory responses (Fig. 2, element 210 – a write cache inherently receives and stores memory responses);

a bypass path adapted to receive downstream memory responses, and operable to pass the downstream memory responses (Fig. 2, element 128 – the memory controller creates a bypass path from the main memory (element 132 not shown in Fig. 2) to the mux (element 220), i.e. downstream, without having to store the memory response in the prefetch buffer;

a buffered queue coupled to the bypass path and operable to store downstream memory responses (Fig. 2, element 126, the prefetch buffer is coupled to the memory controller. Again, a prefetch buffer inherently stores memory responses, in this instance, downstream from the main memory) – col. 5, lines 24-28;

a multiplexer coupled to the local queue, buffered queue and bypass path, the multiplexer being operable to output responses inform a selected one of the queues or the bypass path responsive to a control signal (the mux can output one of the three responses (either from the

prefetch buffer, the bypass path (memory controller) or the write cache) and output it to the processor bus controller (element 114)). A control signal (element 222) is provided from the read request queue (element 214) which selects one of the three aforementioned signals (col. 3, lines 33-43); and

arbitration control logic coupled to the multiplexer, the arbitration logic operable to develop the control signal to control the selection of responses output by the multiplexer (again, the read request queue generates the control signal (222) to select one of the three responses (col. 3, lines 33-43).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Talbot to incorporate Bogin's memory hub into his own system serially connected memory modules including a cache. By doing so, Talbot would benefit having by having a system that could speculatively prefetch memory that is likely to be requested by the processor in the near future, hence improving the system's performance, as taught by Bogin (col. 1, lines 12-24).

As for claim 34, Talbot teaches a computer system, comprising:

a processor (Fig. 1, element 100 – note in Fig.4, element 410 – Talbot teaches the host as being a processor);

a system controller coupled to the processor, the system controller including a memory hub controller (Fig. 105, the controller coupled to the processor acts as a system controller as it used to access the system memory (element 125) – paragraph

0027, lines 1-9. Further the system controller itself acts as a memory hub controller as it accesses the memory control hub in order to access the memory chips in Fig. 2 (i.e., element 216A) – paragraph 0051, lines 1-16);

an input device, and output device, and a storage device coupled to the processor through the system controller (each of the memory modules 150A though 150N (as shown in Fig. 1) are coupled to the system controller (element 105) via memory links. Each of the modules is capable of inputting, outputting and storing data);

a plurality of memory modules (Fig. 1, elements 150A-150B) , each memory module being coupled to adjacent memory modules through respective high-speed links (Fig. 1, elements 110B and110C – paragraph 0034, lines 1-5), at least one of the memory modules being coupled to the memory hub controller through a respective high-speed link (Fig. 1 depicts the high-speed uplink and downlinks (elements 111A and 112A respectively) coupled to the hub controller), and each memory module comprising:

a plurality of memory devices (Fig. 2, element 261A through 261N); and

a memory hub coupled to the memory devices (Fig. 1, element 112).

Though Talbot teaches a memory hub, he fails to teach the memory hub as claimed by Applicant. Bogin however teaches a memory hub comprising,

a local queue adapted to receive local memory responses, and operable to store the local memory responses (Fig. 2, element 210 – a write cache inherently receives and stores memory responses);

a bypass path adapted to receive downstream memory responses, and operable to pass the downstream memory responses (Fig. 2, element 128 – the memory controller creates a bypass path from the main memory (element 132 not shown in Fig. 2) to the mux (element 220), i.e. downstream, without having to store the memory response in the prefetch buffer;

a buffered queue coupled to the bypass path and operable to store downstream memory responses (Fig. 2, element 126, the prefetch buffer is coupled to the memory controller. Again, a prefetch buffer inherently stores memory responses, in this instance, downstream from the main memory) – col. 5, lines 24-28;

a multiplexer coupled to the local queue, buffered queue and bypass path, the multiplexer being operable to output responses inform a selected one of the queues or the bypass path responsive to a control signal (the mux can output one of the three responses (either from the prefetch buffer, the bypass path (memory controller) or the write cache) and output it to the processor bus controller (element 114)). A control signal (element 222) is provided from the read request queue (element 214) which selects one of the three aforementioned signals (col. 3, lines 33-43); and

arbitration control logic coupled to the multiplexer, the arbitration logic operable to develop the control signal to control the selection of responses output by the multiplexer (again, the read request queue generates the control signal (222) to select one of the three responses (col. 3, lines 33-43).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Talbot to incorporate Bogin's memory hub into his own system serially connected memory modules including a cache. By doing so, Talbot would benefit having by having a system that could speculatively prefetch memory that is likely to be requested by the processor in the near future, hence improving the system's performance, as taught by Bogin (col. 1, lines 12-24).

As for claims 26 and 36, Talbot teaches the memory devices as comprising SDRAM (paragraph 0005, lines 10-14).

As for claim 27, Bogin teaches the memory system of claim 24 wherein the arbitration control logic develops the control signal to output memory responses stored in the local queue prior to memory responses stored in the buffered queue (col. 3, lines 24-45, read requests are sent from the processor via the processor bus controller to the read request controller (Fig. 2, element 206). If the read request controller selects an entry in the write cache, the control signal (element 222) will instruct the mux to output the memory responses from the write cache prior to any requests from the prefetch buffer).

As for claim 28, Bogin teaches the memory system of claim 27 wherein the arbitration control logic develops the control signal to output memory responses stored in the buffered queue prior to memory responses stored in the local queue (col. 3, lines 24-45, read requests are sent from the processor via the processor bus controller to the read request controller (Fig. 2, element 206). If the read request controller selects an entry in the prefetch buffer, the control signal (element 222) will instruct the mux to output the memory responses from the prefetch buffer prior to any requests from the write cache).

As for claim 29, Bogin teaches the arbitration control logic as developing the control signal to provide the memory responses from the local and buffered queues as a function of the age of a memory request associated with each memory response (col. 5, lines 48-67, Bogin discusses assigning an age value to each entry in the buffers. The least recently used logic is then implemented to assign ages to the entry, hence limiting the amount of time it can be stored in the buffer before is read out (as selected by the read request controller).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Talbot to incorporate Bogin's memory hub into his own system serially connected memory modules including a cache. By doing so, Talbot would benefit having by having a system that could speculatively prefetch memory that is likely to be requested by the processor in the near future, hence improving the system's performance, as taught by Bogin (col. 1, lines 12-24).

As for claim 37, Talbot teaches the computer system of claim 34 wherein the processor comprises a central processing unit (CPU) – the processor (Fig. 4, element 410) is the only processor, which oversees operation of the computer system (element 400), therefore inherently it is the central processing unit.

13. Claims 16-19 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bogin in further view of Walton et al., hereinafter Walton (US Patent 6,904,556 B2).

As for claim 16, though Bogin doesn't teach his memory devices (i.e. cache) as comprising an SDRAM, it would have been obvious to one of ordinary skill in the art at the time of the invention for Bogin's cache memory to comprise SDRAM in order to exploit the benefits of high-speed access, which is characteristic of such memory. Walton teaches that a cache can be comprised of SDRAM in col. 1, lines 55-62 of his disclosure.

As for claim 17, Bogin teaches the memory module of claim 16 wherein the arbitration control logic develops the control signal to output memory responses stored in the local queue prior to memory responses stored in the buffered queue (col. 3, lines 24-45, read requests are sent from the processor via the processor bus controller to the read request controller (Fig. 2, element 206). If the read request controller selects an entry in the write cache, the control signal (element 222) will instruct the mux to output the memory responses from the write cache prior to any requests from the prefetch buffer).

As for claim 18, Bogin teaches the memory module of claim 17 wherein the arbitration control logic develops the control signal to output memory responses stored in the buffered queue prior to memory responses stored in the local queue (col. 3, lines 24-45, read requests are sent from the processor via the processor bus controller to the read request controller (Fig. 2, element 206). If the read request controller selects an entry in the prefetch buffer, the control signal (element 222) will instruct the mux to output the memory responses from the prefetch buffer prior to any requests from the write cache).

As for claim 19, Bogin teaches the arbitration control logic as developing the control signal to provide the memory responses from the local and buffered queues as a function of the age of a memory request associated with each memory response (col. 5, lines 48-67, Bogin discusses assigning an age value to each entry in the buffers. The least recently used logic is then implemented to assign ages to the entry, hence limiting the amount of time it can be stored in the buffer before is read out (as selected by the read request controller).

As for claims 21, Bogin teaches the memory module of claim 16 wherein the arbitration control logic develops the control signal to alternately output a predetermined number of memory responses stored in the buffered queue and a predetermined number of memory responses stored in the local queue (col. 3, lines 24-43 – the read request controller uses the read request queue to store up to four pending requests. The arbitration logic then can alternatively select read and write requests to output to

the processor bus).

14. Claims 25 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Talbot and Bogin as applied to claims 24 and 34 above, and in further view of Jiang et al., hereinafter Jiang (US Patent 6,947,672 B2).

As for claims 25 and 35, though Talbot teaches using high-speed links to connect his memory modules, he fails to teach the each of the high-speed links comprising an optical communications link. It would have been obvious to one of ordinary skill in the art at the time of the invention for Talbot to include optical communication links as the type of high-speed link to connect his memory modules. By doing so, Talbot would benefit from high transfer rates characteristic of optical communication as taught by Jiang in col.1, lines 49-55 (i.e. 10 Gbps or beyond).

15. Claims 8, 14 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bogin as applied to claims 1 and 15 above, and in further view of Osborne et al., hereinafter Osborne (US PG Publication 2004/0128449 A1).

As for claims 8, 14 and 23, though Bogin fails to teach his memory responses as including a header, Osborne teaches a method and system to improve prefetching operations which includes memory responses comprising data and a header in order to identify a memory request corresponding to the memory response. In his disclosure, Osborne teaches a prefetch component inserting a header in a partial data set. The partial data set is then subsequently

prefetched from the system memory and buffer (paragraphs 0015-0016). Note the header contains memory request information (i.e. transaction type) as claimed by Applicant– paragraph 0017.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Bogin to further include Osborne's system to improve prefetching operations into his own prefetching system. By doing so, Bogin could benefit improving memory latency, by reducing the amount of data that is prefetched beyond what is needed by the system (i.e. overshoot) as taught by Osborne in paragraphs 0001-0002.

16. Claims 33 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Talbot and Bogin as applied to claims 24 and 34 above, and in further view of Osborne.

As for claims 33 and 38, though Talbot fails to teach his memory responses being transmitted between the host and memory modules as including a header, Osborne teaches a method and system to improve prefetching operations which includes memory responses comprising data and a header in order to identify a memory request corresponding to the memory response. In his disclosure, Osborne teaches a prefetch component inserting a header in a partial data set. The partial data set is then subsequently prefetched from the system memory and buffer (paragraphs 0015-0016). Note the header contains

memory request information (i.e. transaction type) as claimed by Applicant–paragraph 0017.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Talbot to further include Osborne's system to improve prefetching operations of his cache operations. By doing so, Talbot could benefit improving memory latency, by reducing the amount of data that is prefetched beyond what is needed by the system (i.e. overshoot) as taught by Osborne in paragraphs 0001-0002.

Allowable Subject Matter

17. Claims 5-7, 20, 22, 30-32 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, and rewritten to overcome the objections set forth under section 10 of this correspondence.

18. The following is a statement of reasons for the indication of allowable subject matter:

As for claims 5, 20 and 30, neither Bogin, nor Talbot teach (either individually or in combination) the memory hub of claim 4 (or module of claim 15, or system of claim 24), wherein the arbitration control logic assigns a time stamp to each memory request when the request is received by the hub, and wherein the age of each request corresponds to the assigned time stamp.

As for claims 22, neither Bogin, nor Talbot teach (either individually or in combination) the memory module of claim 21 wherein the same predetermined number of responses are alternately output from each queue if such predetermined number or a greater number of responses are stored in each queue.

Claims 6-7 further limit claim 5, therefore they to are deemed allowable.

Claims 31 further limits claim 30, therefore they to are deemed allowable

Conclusion

19. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Kapur et al. (US PG Publication 2003/0163649 A1) teaches a shared bypass bus structure.

Radhakrishnan et al. (US PG Publication 2004/0022094 A1) teaches a cache usage for concurrent multiple streams.

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Craig E Walter
Examiner
Art Unit 2188

CEW

12/22/05

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER